

# SG-8018CE 20.00000 MHZ TJHPA EPSON ELECTRONICS AMERICA

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## **Company Address**

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Crystal oscillator

## CRYSTAL OSCILLATOR (Programmable) OUTPUT: CMOS

## SG-8018 series

- Frequency rangeSupply voltage
- e : 0.67 MHz to 170 MHz (1 ppm Step) 1.62 V to 3.63 V
- Function
- : Output enable (OE) or Standby (ST)
- Frequency tolerance : ±50 ppm (-40 °C to +105 °C)

PLL technology to enable short lead time

Available field oscillator programmer "SG-Writer II"

Pb Free RoHS Compliant Product Number SG-8018CG: X1G005601xxxx00 SG-8018CE: X1G005591xxxx00 SG-8018CB: X1G005581xxxx00 SG-8018CA: X1G005571xxxx00





2.5 × 2.0 mm 3.2 × 2.5 mm

5.0 × 3.2 mm 7.0 × 5.0 mm

Specifications (characteristics)									
Item		Symbol	Specifications			Conditions/Remarks			
Supply voltage		Vcc	1.80 V Typ. 2.50 V Typ. 3.30 V Typ.			_	_		
			1.62 V to 1.98 V 1.98 V to 2.20 V 2.20 V to 2.80 V 2.70 V to 3.63 V				-		
Output frequency range		fo	0.67 MHz to 170 MHz						
Storage tempera		T_stg	-40 °C to +125 °C			Storage as single p	roduct.		
Operating tempe		T_use	-40 °C to +105 °C			-			
Frequency tolerance <sup>*1</sup>		f_tol	J: ±50 × 10 <sup>-6</sup>		T_use = -40 °C to +105 °C				
Current concumption		Icc	3.2 mA Max.         3.3 mA Max.         3.4 mA Max.         3.5 mA Max.			T_use = +105 °C	—No load, f <sub>0</sub> = 20 MHz		
			2.7 mA Typ. 2.9 mA Typ. 3.0 mA Typ.			T_use = +25 °C			
Current consum	Current consumption		5.5 mA Max.	5.8 mA Max.	6.7 mA Max.	8.1 mA Max.	T_use = +105 °C	No load, f <sub>0</sub> = 170 MHz	
			4.7 r	nA Typ.	5.7 mA Typ.	6.8 mA Typ.	T_use = +25 °C		
Output disable current		I_dis	3.2 mA Max.	3.2 mA Max.	3.3 mA Max.	3.5 mA Max.	OE = GND, f <sub>0</sub> = 170	) MHz	
Standby current		I std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	ST = GND	
Stanuby current		I_SIU	0.3 µА Тур.	0.4 µА Тур.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C		
Symmetry		SYM	45 % to 55 %		50 % V <sub>CC</sub> Level				
							IOH/IOL Conditions	[mA]	
			90 % V <sub>CC</sub> Min.			Rise/Fall time	V <sub>CC</sub> *A *B *C *D		
		Vон				Default (f <sub>O</sub> > 40 MHz),	I <sub>OH</sub> -2.5 -3.5 -4.0 -5.0		
Output voltage							IoL         2.5         3.5         4.0         5.0           IoH         -1.5         -2.0         -2.5         -3.0		
(DC characterist	tics)						Default (to $\leq 40 \text{ MHz}$ )	$I_{OL}$ 1.5 2.0 2.5 3.0	
,	(2000)						lou		
		Vol	10 % V <sub>CC</sub> Max.			Slow $I_{OL}$ 1.0 1.5 2.0 2.5			
							V to 1.98 V, *B: 1.98 V to 2.20 V,		
		L CMOS					*C: 2.20	V to 2.80 V, *D: 2.70 V to 3.63 V	
Output load condition		-	15 pF Max.					-	
Input voltage		V <sub>IH</sub>	70 % V <sub>CC</sub> Min.				OE or ST		
	1	VIL	30 % V <sub>CC</sub> Max.						
	Default		3.0 ns Max.				f <sub>0</sub> > 40 MHz		
Rise time	Delault	tr/tf	6.0 ns Max.				f <sub>0</sub> ≤40 MHz	20 % - 80 % Vcc,	
/Fall time	Fast	u/u	3.0 ns Max.				f <sub>0</sub> = 0.67 MHz to 17	0 170 MHz L_CMOS = 15 pF	
	Slow		10.0 ns Max.				f <sub>0</sub> = 0.67 MHz to 20	.o 20 MHz	
Output disable time (OE)		tstp_oe	1 µs Max.				time OE or ST pin crosses 30 %		
Output disable time (ST)		tstp_st	•			Vcc			
Output enable time (OE)		tsta_oe	1 μs Max.				time OE pin crosses 70 % V <sub>CC</sub>		
Output enable time (ST)		tsta_st	3 ms Max.				time ST pin crosses 70 % V <sub>CC</sub>		
Start-up time		t_str	3 ms Max.			Measured from the minimum value, 1.6	time V <sub>CC</sub> reaches its rated 2 V		
Frequency aging	Frequency aging		This is included in frequency tolerance specification.			+25 °C, 10 years			

 Frequency aging
 f\_age
 This is included in frequency tolerance specification.
 +25 °C, 10 years

 \*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 10 years).

Pin description								
Pin	Name	I/O type		Function				
	OE	Input	Output enable	High <sup>*2</sup> : Specified frequency output from OUT pin				
	0E	input		Low: Out pin is low (weak pull down), only output driver is disabled.				
1		Input	Standby	High <sup>*2</sup> : Specified frequency output from OUT pin				
	ST			Low: Out pin is low (weak pull down),				
				Device goes to standby mode. Supply current reduces to the least as I_std.				
2	GND	Power	Ground					
3	OUT	Output	Clock output					
4	V <sub>cc</sub>	Power	Power supply					

\*2 Please do not use the OE/ST terminal in the open state.

#### SEIKO EPSON CORPORATION



In order to achieve optimum jitter performance, the 0.1 µF capacitor between V<sub>CC</sub> and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

## PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

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All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

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